

■ Silicon Problems

Problem	Probable Cause	Suggested Solution	Comments
Silicon	* Excessive glass transfer * Residual photo-	* Use correct source for deposition temp. * Use "RCA Clean"	* Brochure * (7) * (8hgs.

- (6) The use of 1/4" oversize sources was fairly common when silicon wafers were only 2" in diameter. However, oversize sources are rarely used when the silicon wafers are more than 3" in diameter.
- (7) If it is felt that too much B₂O₃ or P₂O₅ is being deposited on a silicon wafer during a deposition cycle, it is sometimes possible to use different BoronPlus or PhosPlus sources to obtain less glass. For example, both the GS-139 and GS-245 sources can be used over the 1050-1075°C temperature range (see BoronPlus Brochure). Changing from the GS-139 source to the GS-245 source when doping the silicon within this temperature range will result in essentially the same sheet resistivity, but a significant reduction in the thickness of the deposited glass will be observed.
- (8) Silicon wafers should be given the "RCA Clean" [1] immediately after removal of the photoresist. If a significant time is allowed to elapse before they are cleaned, the residual photoresist will harden, and it will be difficult, if not impossible, to remove. The resist will eventually react with the silicon surface during diffusion resulting in the creation of damage sites.
- (9) If the deposited boron glassy film is more than about 500 Å, its surface becomes very hygroscopic, and the silicon quickly absorbs moisture from the room air. In severe cases, the absorbed moisture can be easily detected by the development of a milky appearance. If the silicon slices are inserted back into the diffusion furnace for further processing with this absorbed moisture, boric acid crystals (HBO₂) will form. The crystals will damage the silicon and penetrate deep into the field oxide causing additional processing problems. Moisture absorption can be prevented by (a) keeping the silicon wafers dry, (b) immediately etching off the deposited glass in dilute HF, or (c) rinsing the silicon slices in DI water immediately after they are removed from the diffusion furnace. The DI water rinse apparently washes away the hygroscopic surface of the deposited glass and prevents absorption of moisture. Experience has shown that either the acid etch or the DI water rinse must be done before the milky surface forms or it will not come off. A permanent "footprint" will be left behind that will eventually damage the silicon surface or field oxide.
- (10) Normally, oxygen is included in the nitrogen carrier gas to prevent silicon surface damage. However, if the oxygen level is decreased far enough, a small number of damage sites can be purposely introduced into the silicon. These sites will tend to getter unwanted impurities in the silicon wafer with a resulting increase in the minority carrier lifetime.
- (11) Tests have shown that aging the GS-139 BoronPlus sources at 1075°C for about 16 hours will result in a significant increase in the minority carrier lifetime for subsequent depositions [2]. Somewhat longer aging times would be required to observe the same effect at lower use temperatures.
- (12) A systematic study on silicon wafers doped with BoronPlus sources has shown that low minority carrier lifetimes may be caused by deep level defects originating from high concentrations of boron atoms at the silicon surface [3]. Slowly annealing the silicon wafers from a temperature above 700°C anneals out these defects and the minority carrier lifetime is increased.
- (13) It has been reported that if the TP470 PhosPlus sources are allowed to remain out of the diffusion furnace for several hours, the next emitter diffusion will sometimes produce higher betas of the transistor. This may be caused by slight moisture absorption of the sources resulting in increased P₂O₅ evolution rate. The higher rate results in decreased base width and a higher beta of the transistor. This can be avoided by minimizing source time outside of the diffusion furnace. The sources can be restored back to their original performance by reinserting them into the diffusion furnace at the insertion temperature for about 15 min.

For more information on this Product Bulletin or on the BoronPlus and PhosPlus dopant sources, contact the Planar Dopants Team: www.techneglas.com

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References:

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2. Hur-Ling Hsiu, "Effect of Solid Source Impurities on Silicon Devices", Thesis at Arizona State University, Dec. 1988.
3. "Processed-Induced Defects in Borosilicate Glass-Diffused Silicon", O. Aina and R. Kennedy, J. Electrochem. Soc., vol. 131, no. 8, pp 1884-1887.
4. J.E. Rapp, "The Planar Diffusion Technique", Semicon Technology Asia 1998/9, Nordica International. 3.F Block B, Quarry Bay, Hong Kong, p.33.
5. T.A. Carbone, "Solid Source Doping of a Double Polysilicon Capacitor", Semiconductor International, Nov. (1997) p. 89-95.
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